

Figure 1

Figure 3

	DST	1 1 1 1 1	BASE REG	<u>-</u>	INDX REG	INDX OP T	_	OPCODE	<u> </u>
<u>(</u>	DST	_	BASE REG	-	IMMEDIATE OFFSET	IMMEDIA	- T	OPCODE	3
<u>®</u>	DST		SRC1	<u> </u>	SRC2	s TST	 	OPCODE	H G
(4)	DST	-	SRC1	-	SHIFT M REG		 . 	OPCODE	м — —
(3)	M REG (3)	SIGN	SRC1	<u> </u>	SRC2	S TST	 	OPCODE	M G
(2)	DST	- -	SRC1	<u> </u>	IMMED	TST	 	OPCODE	M G
(1)	DST		SRC1	-	src2	S TST	i t t t i t	OPCODE	M G
)3 02 01 00	06 05 04 0	10 09 08 07 0	12 11	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	21 20 19 1	24 23 22	29 28 27 26 25	31 30
		 	: : : : : : : : : : : : : : : : : : :	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 2 2 2 2 3 3 4 4 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	 	* 1	4
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Figure 26

bit	31 (M)	30 (G)	29 (G)
register/immediate	1	0	X
register/register	1	1	0
MAC operations	1	1	1

FIGURE 4

-63	-62	-5350	-49-44	43-38	3-3732	2-31-2	9-2818	8-17-12				
	Operation	Branc	h conc	lition	Immed	111	Immediat	te 		Reg		L1
10	Operation	s TST	Src4	Src3	Dest2	111	Reserved	Src2	Src1	Dest1	_ [٨2
10	Operation	S TST	Immed	liate 🕨	116	1111	Immediate	ا 16انتها	Src1	Dest1		L3

Figure 5